UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,583	12/20/2001	Theodore I. Kamins	10018774-1	4949

7590 10/22/2003

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
MCDONALD, RODNEY GLENN	

ART UNIT	PAPER NUMBER
1753	

5

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/029,583	KAMINS ET AL.
	Examin r	Art Unit
	Rodney G. McDonald	1753

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2, 5, 7, 8, 10-13 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. (U.S. Pat. 6,379,572) in view of Deckman et al. (U.S. Pat. 4,407,695).

Kikuchi et al. teach in FIGS. 6A & 6B, therein are shown a cross-sectional side view and a top view of ***the insulator 20 (i.e. substrate) (The insulator can be silicon dioxide.*** See Column 4 lines 1-3) and the conductive gate electrode 22 with ***a soft mask material 60*** deposited on the conductive gate electrode 22. ***The soft mask***

material 60 may be of a number of different materials, such as a silicon nitride (SiN). The same numbers are used here to designate the same elements as in the PRIOR ART. Generally there is a cleaning step before deposition of the soft mask material 60 to assure good contact between the soft mask material 60 and the gate electrode 22. (Column 4 lines 57-68)

Referring now to FIGS. 7A & 7B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 6A & 6B ***with microspheres 50-52 deposited on the soft mask material 60.*** Again, the microspheres 51 and 52 are in contact. (Column 5 lines 1-5)

Referring now to FIGS. 8A & 8B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 7A & 7B after ***etching of the soft mask material 60 and before removal of the microspheres 50-52***. During etching of the soft mask material 60, the soft mask material 60 is etched in areas away from the microspheres 50-52 and also undercuts the microspheres 50-52. For example, where the microsphere 50 has a diameter equal to A, the area A under the microsphere 50 will be etched away to have a diameter designated by the letter B. The undercutting leaves soft mask portions 61-63 of the soft mask material 60. As shown in FIG. 8B, the remaining portion soft mask material 60 is removed until a large portion of the conductive gate electrode 22 is exposed. (Column 5 lines 6-19)

Referring now to FIGS. 9A & 9B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 8A & 8B ***after the microspheres 50-52 are removed and a deposition of a hard mask material 64.*** The microspheres

50-52 may be removed by megasonic cleaning or by a process, such as ashing, to burn up the microspheres 50-52 followed by a cleaning process to remove the ash. ***The hard mask material covers the soft mask portions 61-63. The hard mask material 64 may be of a material such as spin-on glass (SOG)***, which is permitted to level out and then is baked to form a hard coating over the soft mask portions 61-63 and the conductive gate electrode 22. (Column 5 lines 20-32)

Referring now to FIGS. 10A & 10B, therein are shown a cross-sectional side view and a top view of the respective structures of FIGS. 9A & 9B ***after chemical mechanical polishing (CMP) to remove the hard mask material 64 until the soft mask portions 61-63 are exposed. Alternatively, an etch-back process is used with an etch having selectivity to the soft mask material 60 of the soft mask portions 61-63. FIGS. 10A & 10B also show removal of the soft mask portions 61-63 by isotropic etching to leave the hard mask material 64 with holes 66-68 which expose the conductive gate electrode 22.*** (Column 5 lines 33-43)

The first mask material can be selected from a group consisting of silicon nitride, silicon oxynitride, and combinations thereof. (Column 6 lines 18-20)

The microspheres can be made of a material selected from silica, glass, plastics, and a combination thereof. (Column 6 lines 30-33)

The second mask can be selected from a material of spun on glass, silicon dioxide and a combination thereof. (Column 6 lines 39-40)

The differences between Kikuchi et al. and the present claims is that utilizing nanoparticles is not discussed and reactive ion etching is not discussed.

Deckman et al. teach directional ion etching to form microcolumnar structures. (See Abstract) Deckman et al. teach coating a substrate with a monolayer of colloidal particles substantially over the entire surface such that the particles are fixed to the substrate in a predetermined way as to particle size distribution and mean distance between particles, the monolayer of colloidal particles serving as an etch mask for forming an etched pattern in the substrate. (Column 8 lines 19-26)

The etching is performed with a reactive plasma with an ion beam. (Column 8 lines 31-38; Column 7 lines 17-19)

Monodispheres in the range of 200 Angstroms ***(i.e. 20 nm)*** to 40 m can be utilized as the mask. (Column 5 lines 7-10) ***(Utilizing the low end of the range will result in Applicant's required nanopore)***

Spheres of 500 Angstroms ***(i.e. 50 nm)*** to 20 microns can be utilized as the mask. (Column 4 lines 35-36) ***(Utilizing the low end of the range will result in Applicant's nanopore)***

The structures to be fabricated can be as small as 50 angstroms. (Column 6 lines 29)

Islands of a silver film can be used as the mask of 50 Angstroms ***(i.e. 5 nm)*** in dimension. (Column 6 lines 40) ***(Utilizing 50 Angstrom mask will result in Applicant's nanopore)***

The motivation for utilizing nanoparticles and reactive ion etching is that it allows deposition of a large are lithographic mask on the surface of a substrate. (Column 2 lines 20-22)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Kikuchi et al. by utilizing nanoparticles of a particular size that will produce holes of a particular size and reactive ion etching as taught by Deckman et al. because it allows for producing a large area lithographic mask on the surface of a substrate.

Claims 3, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. in view of Deckman et al. as applied to claims 1-2, 5, 7, 8, 10-13 and 23 above, and further in view of Hatakeyama et al. (U.S. Pat. 6,010,831).

The differences not yet discussed is the size of the nanoparticles in the range of 1 to 10 nm is not discussed and the sizes of the holes is not discussed.

Hatakeyama et al. teach utilizing ***nanometer*** or micrometer ***sized microparticles*** to produce a variety of three-dimensional fine structures which have not been possible by the traditional photolithographic technique. An energy beam with reactive gas particle beam can be used to produce the fine structures. (See Abstract)

It is an object of Hatakeyama et al.'s invention to provide a method of energy beam assisted ultra-fine microfabrication to enable fabrication of fine structures in a nanometer range by dispersing micro-particles as beam shielding means on a fabrication surface of a target object. (Column 2 lines 20-24)

The first object is achieved by dispersing and ***position micro-particles having particle sizes in ranges of one of from 1-10 nm***, 2 from 10-100 nm and 2 from 100 nm to 10 micrometers for shielding regions of a fabrication surface of a target object

from exposure to an energy beam, and radiating the energy beam on the fabrication surface so as to produce a fine structure by an etching action. (Column 2 lines 41-49)

The target object may be silicon dioxide. (Column 4 lines 27-30)

The width of the fine pattern elements can have a width of 0.1-100 nm. The depth can be between 0.1- 100 nm. (Column 12 lines 61-64)

The motivation for utilizing nanoparticles of a particular size that will produce holes of a particular size is that it allows for reaching dimensions that photolithographic techniques cannot reach. (See Abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized nanoparticles in the range of 1 to 10 nm and developed a particular size of holes as taught by Hatakeyama et al. because it allows for reaching dimensions that photolithographic techniques cannot reach.

Claims 9, 14-20, 24-26 and 28-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. in view of Deckman et al. and further in view of Hatakeyama et al. as applied to claims 1-3, 5, 7, 8, 10-13 and 21-23 above, and further in view of Jun et al. (U.S. Pat. 5,393,373).

The differences not yet discussed is utilizing CVD to deposit the insulating material, depositing material in the nanopore, utilizing an electrical substrate of doped polycrystalline silicon, a tunnel barrier and the material being is semiconductive.

Jun et al. teach ***depositing insulation material by CVD***. (Column 6 lines 9-11)

Jun et al. teach in FIGS. 8a to 8e are schematic sectional views for explaining a method of manufacturing capacitors of semiconductor devices in accordance with the second embodiment of the present invention. (Column 6 lines 63-66)

In this method, oxide layer 12 is first coated on semiconductor substrate 11 on which a transistor (not shown) has been previously formed. In oxide layer 12, capacitor node contacts are then formed. Thereafter, ***doped polysilicon layer 24*** is coated on the overall surface of oxide layer 12 to form a plug, as shown in FIG. 8a. ***Insulation layer 25*** such as an oxide layer is then coated on the overall surface of polysilicon layer 24. ***On insulation layer 25, hemisphere particle layer 14 of polysilicon is coated to have alternating hills and valleys, as shown in FIG. 8b.*** (Column 6 lines 67-68; Column 7 lines 1-9)

The portions of insulation layer 25 disposed beneath the valley portions of hemisphere particle layer 14 are then etched back to expose partially polysilicon layer 24, by using the hill portions of hemisphere particle layer 14 as a pattern mask. As a result, insulation layer 25 has a plurality of protrusions thereon, as shown in FIG. 8c. (Column 7 lines 10-16)

Thereafter, ***another doped polysilicon layer 26 is coated on insulation layer 25 to fill valleys thereof and cover the protrusions thereof. Polysilicon layer 26 is then etched back to expose the upper surface of insulation layer 25, as shown in FIG. 8d.*** (Column 7 lines 17-21)

Insulation layer 25 is removed to expose the upper surface of polysilicon layer 24. ***Subsequently, dielectric layer 16 and plate polysilicon layer 17 are coated in***

turn on the overall upper surface of polysilicon layers 24 and 26 to produce a capacitor, as shown in FIG. 8e. (Column 7 lines 23-27)

The motivation for utilizing CVD to deposit the insulating material, depositing material in the nanopore, utilizing an electrical substrate of doped polycrystalline silicon, a tunnel barrier layer and the material being semiconductive is that it allows for production of a semiconductor device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized CVD to deposit the insulating material, to have deposited material in the nanopore, to have utilized an electrical substrate of doped polycrystalline silicon, to have utilized a tunnel barrier layer and top have utilized a semicondcutive material as taught by Jun et al. is that it allows for production of a semiconductor device.

Claims 4 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. in view of Deckman et al. further in view of Hatakeyama et al. and further in view of Jun et al. as applied to claims 1-3, 5-26 and 28-46 above, and further in view of Brandes et al. (U.S. Pat. 5,900,301).

The differences not yet discussed is the particle being inorganic coated with an organic.

Brandes et al. teach applying carbon particles for etching. The particles are applied through an organic solvent. (Column 9 lines 21-59)

The motivation for utilizing a particle that is inorganic coated with an organic is that it allows for developing pillars when anisotropic etching takes place. (See Figure 6C)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have utilized a particle being inorganic coated with an organic as taught by Brandes et al. because it allows for the development of pillars when etching.

Response to Arguments

Applicant's arguments filed July 30, 2003 have been fully considered but they are not persuasive.

In response to the argument that there is no suggestion from the combination of Kikuchi et al. and Hatakeyama et al. to utilize reactive ion etching, it is argued that the newly cited reference to Deckman et al. suggest utilizing reactive ion etching to form nanopores utilizing particle sizes of 20 nm (200 Angstroms), 50 nm (500 Angstroms) and 5 nm (50 Angstroms). (See Deckman et al. discussed above)

In response to the argument that Jun et al. does not suggest disposing at least one molecule in a nanopore, it is argued that Jun et al.'s process would necessarily deposit at least one molecule in a nanopore if the substrate had the nanopore and if the deposition process was carried out thereon. (See Jun et al. discussed above)

This action will be made NON-Final to give Applicant an opportunity to respond to the newly cited reference to Deckman et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rodney G. McDonald whose telephone number is 703-308-3807. The examiner can normally be reached on M- Th with Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam X. Nguyen can be reached on 703-308-3322. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Rodney G. McDonald
Primary Examiner
Art Unit 1753

RM
October 16, 2003